

### REMARKS

In the Official Action mailed **June 5, 2002**, the Examiner reviewed claims 1-7, 9-16, and 18-20. Claims 1-5, 7, 10, 12, and 20 were rejected under 35 U.S.C. §103(a), as being unpatentable over Dea (USPN 5,469,208, hereinafter "Dea") in view of Potu (USPN 5,859,651, hereinafter "Potu"). Claims 6, and 13-16 were rejected under 35 U.S.C. 103(a) as being unpatentable over Dea and Potu and further in view of Abramatic et al. (USPN 4,546,383, hereinafter "Abramatic"). Claim 9 was rejected under 35 U.S.C. 103(a) as being unpatentable over Dea and Potu in view of Yan (USPN 5,438,374, hereinafter "Yan"). Claim 11 was rejected under 35 U.S.C. 103(a) as being unpatentable over Dea and Potu in view of Hardiman (USPN 5,923,223, hereinafter "Hardiman"). Claim 18 was rejected under 35 U.S.C. 103(a) as being unpatentable over the system of Dea, Potu and Abramatic as applied to claim 13, and further in view of Yan. Claim 19 was rejected under 35 U.S.C. 103(a) as being unpatentable over the system of Dea, Potu and Abramatic as applied to claim 13, and further in view of Hardiman.

#### Rejections under 35 U.S.C. §103(a)

Independent claim 1 and 20 were rejected as being unpatentable over Dea in view of Potu and independent claim 13 was rejected as being unpatentable over Dea and Potu and further in view of Abramatic. Applicant respectfully points out that Dea is directed to a compression/decompression accelerator **coupled to a system bus** (See Dea, Fig. 1). In contrast, the present invention discloses a graphics controller **within a core logic unit, which includes the circuitry of the north bridge chip** (See Fig. 2, and page 8, lines 4-6 of the instant application and also page 8, line 5 of the instant application). A core logic unit is circuitry within a computer system that interfaces a processor to a memory and a peripheral bus and performs other functions (See page 5, lines 12-13 of the instant application).

The north bridge chip is well known in the art and was well known in the art at the time of the invention. The north bridge chip provides coupling logic to the various peripherals within a computer system and alleviates bus contention when accessing these peripherals because the signals remain within the north bridge chip.

Including the graphics controller with the north bridge chip circuitry within the core logic unit is advantageous because communications between the graphic controller and the core logic elements remain within the core logic unit and are therefore faster than when these communications pass through a system bus. Performing these communications across the system bus is slower because system bus bandwidth is typically less than the bandwidth within the north bridge chip, and because of system bus contention with other peripheral devices. There is no suggestion, either explicit or implicit, within Dea, or within Dea in combination with Potu and Abramatic, to include the graphics controller within the north bridge chip.

In the Official Action mailed **June 5, 2002**, the Examiner states “the limitation of wherein the apparatus reside as a core logic circuit for a computer system as described by the compress/decompression accelerator 120 that includes the function frame difference block 220 (column 6, lines 36-44, and column 5, lines 42-47, and FIG. 1 and 2), where the description at column 5 and Fig. 2 elucidated the compressor/decompressor 120 is a circuitry within the video interface system that interface with the processor 112 to the RAM by way of accelerator bus interface.”

Applicant respectfully points out that frame difference block 220 of Dea is equivalent to XOR unit 308 (see Dea FIG. 2 and column 6, lines 36-44 and the instant application FIG. 3, and page 9, lines 21-24) and that compression/decompression accelerator 120 of Dea is equivalent to graphics controller 106 of the instant application (see Dea FIG. 1 and column 4, lines 17-19

and the instant application FIG. 2 and page 8, lines 4-6). The remote video processing system 100 of Dea includes separate devices, including compression/decompression accelerator 120, to perform the functions of video processing. This requires communication across the external bus logic (see Dea FIG.1 and column 4 line 17 to column 5, line 37). In contrast, the instant application claims graphics controller 106 embedded within the north bridge chip thereby providing a faster, higher bandwidth path for the graphic signals (see the instant application FIG. 3 and page 8, lines 23-25).

Accordingly, Applicant has amended independent claims 1, 13, and 20 to clarify that the graphics controller is included within the north bridge chip. Dependent claims 8 and 17 were previously cancelled without prejudice.

Hence, Applicant respectfully submits that independent claims 1, 13, and 20 as presently amended are in condition for allowance, and that claims 2-7 and 9-12, which depend upon claim 1, and claims 14-16 and 18-19, which depend on claim 13, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

**Version with markings to show changes made**

**The claims:**

1           1. (Thrice Amended) An apparatus for compressing video data,  
2    comprising:  
3           a video input port, for receiving video data for a current video frame;  
4           a video input buffer coupled to the video input port, for storing video data  
5    from the video input port;  
6           a previous frame buffer, for storing at least a portion of a previous video  
7    frame;  
8           an operation unit coupled to the video input buffer and the previous frame  
9    buffer, for performing an operation between data from the video input buffer and  
10   data from the previous frame buffer; and  
11          a result buffer coupled to the operation unit, for storing the result of an  
12   operation from the operation unit;  
13          wherein the apparatus resides inside of a north bridge [core logic ]chip for  
14   a computer system so that graphic signals are provided with a higher bandwidth  
15   pathway to improve throughput.

1           13. (Thrice Amended) An apparatus for compressing video data,  
2    comprising:  
3           a video input port, for receiving video data for a current video frame;  
4           a video input buffer coupled to the video input port, for storing video data  
5    from the video input port;  
6           a previous frame buffer, for storing at least a portion of a previous video  
7    frame;

8           an exclusive-OR unit coupled to the video input buffer and the previous  
9 frame buffer, for performing an exclusive-OR operation between data from the  
10 video input buffer and data from the previous frame buffer;  
11           a result buffer coupled to the operation unit, for storing the result of an  
12 operation from the operation unit;  
13           a memory port coupled to the previous frame buffer and the result buffer,  
14 for transferring data to and from a memory that stores video data from the video  
15 input port and result data from the result buffer; and  
16           a memory coupled to the memory port for storing the video data from the  
17 video input port and result data from the result buffer, wherein the video data is  
18 stored to in a current frame in the memory and the result data is stored in a  
19 difference frame in the memory;  
20           wherein the apparatus resides inside of a north bridge [core logic ]chip for  
21 a computer system so that graphic signals are provided with a higher bandwidth  
22 pathway to improve throughput.

1           20. (Thrice Amended) A computer system including resources for  
2 compressing video, comprising:  
3           a central processing unit within the computer system;  
4           a video input port, for receiving video data for a current video frame;  
5           a video input buffer coupled to the video input port, for storing video data  
6 from the video input port;  
7           a previous frame buffer, for storing at least a portion of a previous video  
8 frame;  
9           an operation unit coupled to the video input buffer and the previous frame  
10 buffer, for performing an operation between data from the video input buffer and  
11 data from the previous frame buffer; and

1           a result buffer coupled to the operation unit, for storing the result of an  
2 operation from the operation unit;  
3           wherein the video input port, the video input buffer, the previous frame  
4 buffer, the operation unit, and the result buffer reside inside of a north bridge  
5 [core logic ]chip for a computer system so that graphic signals are provided with a  
6 higher bandwidth pathway to improve throughput.

**CONCLUSION**

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

By



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